REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-16, 18 and 22 are in the case. No amendments are presented in this document.

Applicants acknowledge with appreciation the allowance of Claims 1-16.

Regarding the rejection of Claims 18 and 22 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Park et al. in view of Microelectronic Circuits, this rejection is respectfully traversed. Claim 18 recites an integrated circuit including a first source region that is shared by a first device comprising the first source region, a first drain region, a first channel region, a first gate and a first drain region, and a second device comprising a second channel region a second gate and a second drain, and including an input/output pad electrically coupled to the first gate and to the second drain region. Note that a "first device" and a "second device" are not explicitly recited, but are inferred from the constituent elements that are recited, and the reference to devices simplifies discussion. The arguments that follow do not depend on the recitation of "first device" or "second device".

The novel structure recited in Claim 18, an embodiment of which is shown, e.g., at the top of Fig. 4A of the instant Specification, provides improved ESD protection for an input device. In Claim 18 the recitation is of a single ended structure connectable to, e.g., ground or to supply voltage, while Figure 4A shows a structure in which two of the structures recited in Claim 18 are connected to the I/O, with protection being provided both with respect to power supply and to ground as a consequence of the use of two such structures. Claim 22 recites a method for forming a structure having a first drain region, a first source region, a second drain region, a first gate, and an input/output pad electrically coupled to the first gate and to the second drain region. Thus, in both claims an input/output pad is connected to a first gate and a second drain region, wherein there is a common source, in order to provide the described beneficial ESD properties.

The patent to Park et al. apparently relates to a semiconductor device fabrication method which is intended to minimize or prevent unreliable silicidation on a narrow active region. Shown in Fig. 6 of that patent is a cross section of what the patent refers to as "an N-channel MOS transistor," apparently having multiple instances of some elements. It is alleged that region 106 therein is a source region shared by two devices. It is respectfully submitted that such allegation is inconsistent with the words of the patent. However, even if such were the case, which Applicants respectfully dispute, nonetheless it was admitted in the above-identified Office Action that Park et al. do not disclose a pad connecting a first gate to a second drain. Applicants add that Park et al. do not suggest such a pad or connection, nor do Park et al. have in their disclosure any motivation to do so, they being concerned with a fabrication process to minimize or prevent unreliable silicidation on a narrow active region, and not with an improved ESD structure or method for making same. Accordingly, Park et al. neither show nor suggest what is set forth in Claim 18 nor what is set forth in Claim 22.

The excerpt from the book Microelectronic Circuits (hereinafter the "Excerpt"), fails to cure the deficiencies of the patent to Park et al. The Excerpt apparently relates to structures using the metal semiconductor field effect transistor ("MESFET"), a semiconductor device having a Schottky metal gate for controlling source to drain current. One of those structures, shown in Fig. 6.43(a), uses two MESFETs connected together to form a composite MESFET, in order to overcome a severe limitation on the performance of a single MESFET, due to its low output resistance. Actually, several of such structures are shown in the Excerpt. The structure shown in Fig. 6.43(a) is a composite MESFET wherein the two MESFETs are connected together in such a way as to form a current source. In that structure the gates of both MESFETs are connected to the source of one of those MESFETs (Q1), the two MESFETs Q1 and Q2 being connected together at the source of Q2 and drain of Q1. In this way a current source is provided, wherein the common connection node of the gates and the source of Q1 forms the source of the composite MESFET.

Nowhere in the Excerpt is any mention made of any ESD problem to be overcome, much less of any solution to any ESD problem. Significantly, the Excerpt does not show an input/output pad connecting a first gate to a second drain, wherein a single source region is used as a common source by a first and second device, as required by Claims 18 and 22. Additionally, the Excerpt itself states that the composite MESFET circuit "is unique to GaAs MESFETs and works only because of the early-saturation phenomenon observed in these devices." (See the first paragraph on page 547 of the Excerpt.) Thus, by the very teaching of the Excerpt there is no motivation to apply its teachings outside of the area of MESFETs, indeed even outside of the area of GaAs MESFETs. The structure shown in Fig. 6 of Park et al. uses no MESFET, but is rather an N-channel MOS transistor. Therefore, there is no teaching, suggestion or motivation in either of these references to combine the teachings of these references in any way for any purpose, including that of forming the structure of Claim 18 or of performing the method of Claim 22. Rather, the Excerpt teaches away from combining it with teachings outside of the area of GaAs MESFETs.

Therefore, it is respectfully submitted that the patent to Park et al. and the Excerpt, whether considered alone or in combination, neither show nor suggest the invention as set forth in Claim 18 and as set forth in Claim 22, and so those claims are allowable over those references. The other art of record is even less relevant.

Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

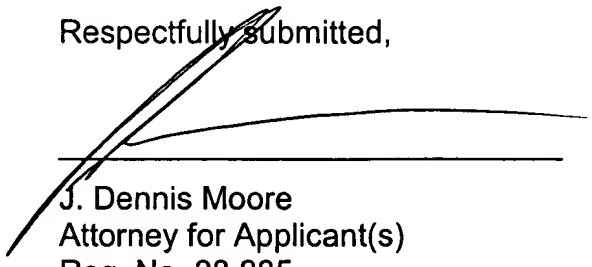
It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or

suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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